## Nathan D. Tuck


Contact Information

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Summary

A self-starting software engineer with strong interests in computer architecture, hardware/software intersections, complex systems problems, and performance. Interested in the big picture as well as the details of building and delivering technology products.

Software Skills

C, C++, Antlr, OpenGL, Perl, Python, Verilog, lex/yacc, RISC assembly (MIPS/ARM/PPC), Linux, Boost, SystemC, VTune, CTM, Valgrind. Some CORBA, Fortran, SQL, HTML, and VHDL.

CAD Tool Experience

VCS, NCSim, SuperFinSim, various Artisan memory compilers, and parts of the Synopsys and Cadence toolchains (mostly simulation and PLI, but some synthesis).

Industrial Experience

**PeakStream** (2/06-5/07) Redwood Shores, CA MTS/Lead

Was one of the lead engineers on a project that built an API and virtual machine targeted at HPC applications. The backend of the virtual machine runs on ATI's R580 and x86 multicore processors. Wrote much of the R580 interface code, and various pieces of the VM infrastructure and API.

**ATI** (8/05-1/06) Santa Clara, CA Contractor

Design verification of the shader control block of the R600 using internal tools and chip-level APIs. Extended existing tools and libraries where they were insufficient.

**SSOC** (1/03-1/06) Pleasanton, CA Founder

Co-founded a company to build a coherent vector coprocessor with a serial memory interface. Funded the company with an R&D contract from AMD and grew it to 8 part-time and and full-time contributors. Wrote specifications for ISA and architecture, and a performance simulator. Built business case and pitched the product to government and industry partners. Filed patents on major innovations.

**Qualcomm** (9/03-12/03) San Diego, CA Consultant

Advised Qualcomm on aspects of their graphics architecture for the MSM6550 and MSM7500 chipsets. Put together verification tools for driving existing OpenGL applications through OpenGL ES hardware.

**Clearwater Networks** (4/01-9/01) San Jose, CA Contractor

Design verification for a simultaneous multithreaded MIPS compatible processor. Assembly, simulator and DV environment work.

**Hotrail/Conexant Inc** (9/99-4/01) San Jose, CA Senior MTS

Design verification for a multiprocessor chip set and an OC-192 switch fabric.

**Raycer Graphics** (6/97-9/99) Palo Alto, CA MTS

Wrote large parts of a C++ simulator for a PC graphics chip set. Also wrote some of the architecture docs and participated in the patent process. Represented the company at standards meetings.

**Silicon Graphics** (5/95-6/97) Mountain View, CA. MTS

Started in technical marketing and performance analysis. Later moved to engineering to do debug and bringup of graphics drivers. Kernel and userland library work.

**Novell** (5/94-9/94) Walnut Creek, CA Intern

Improved stress-testing applications for Novell's AppleTalk protocol stack.

## Education

**University of California**, Department of Computer Science San Diego, La Jolla, CA
Attended various graduate classes in UCSD's Computer Science department through 2001. Admitted to the PhD program in 2002. Completed all technical requirements for an MS. Taught a recitation section in undergraduate architecture in 2002.

**Harvey Mudd College**, Claremont, CA
B.S. Computer Science, May 1996

## Technical Interests

Computer architecture, interactive computer graphics, theory of computation, operating systems, compilers, EDA algorithms, clock tree synthesis algorithms.

## Publications

Multithreaded Value Prediction, Nathan Tuck, Dean M. Tullsen, Presented at the 11th International Symposium on High Performance Computer Architecture, San Francisco, February 2005.

Hardware and Binary Modification Support for Code Pointer Protection From Buffer Overflow , Nathan Tuck, Brad Calder and George Varghese, Presented at 37th International Symposium on Microarchitecture, Portland Oregon, December 2004.

Deterministic Memory-Efficient String Matching Algorithms for Intrusion Detection. Nathan Tuck, Timothy Sherwood, Brad Calder, George Varghese. Presented at Infocom, Hong Kong, 2004.

Initial Observations of a Simultaneous Multithreaded Processor. Nathan Tuck and Dean Tullsen. Presented at the Twelfth International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2003

## Granted Patents

6,771,264 Method and apparatus for performing tangent space lighting and bump mapping in a deferred shading graphics processor.

6,717,576 Deferred shading graphics pipeline processor having advanced features.

6,597,363 Graphics processor with deferred shading.

6,268,875 Deferred shading graphics pipeline processor

6,229,553 Deferred shading graphics pipeline processor

At least 3 other patents in submission.

## References

Available on Request